

**DESCRIPTION**

The STP4407 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

**STP4407**

**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-2.5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$ $T_J=55^\circ C$	$V_{DS}=-30V, V_{GS}=0V$			-1	uA
		$V_{DS}=-30V, V_{GS}=0V$			-5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$		15	20	mΩ
		$V_{GS}=-4.5V, I_D=-6.0A$		24	32	
Forward Transconductance	$g_{fs}$	$V_{DS}=-5V, I_D=-10A$		26		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1.0A, V_{GS}=0V$			-1	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		30		nC
Gate-Source Charge	$Q_{gs}$			4.3		
Gate-Drain Charge	$Q_{gd}$			10		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		2076	2500	pF
Output Capacitance	$C_{oss}$			400		
Reverse Transfer Capacitance	$C_{rss}$			302		
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DD}=15V, R_L=1.25\Omega$ $I_D=-1A, V_{GEN}=-10V$ $R_G=3\Omega$		10.4		nS
				24		
Turn-Off Time	$t_{d(off)}$ $t_f$			12.6		
				12		

**TYPICAL CHARACTERISTICS**

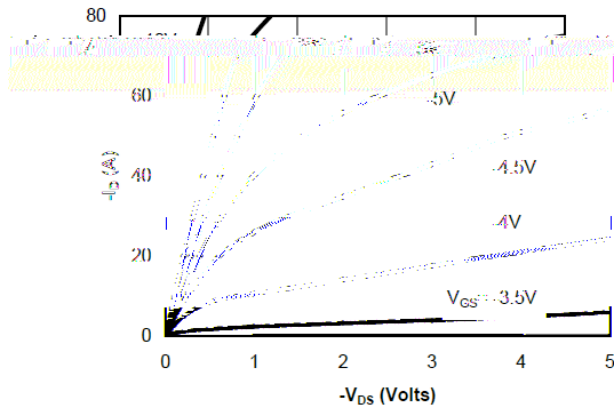


Figure 1: On-Region Characteristics

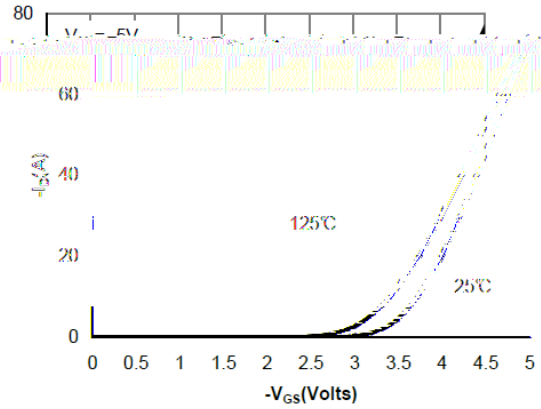


Figure 2: Transfer Characteristics

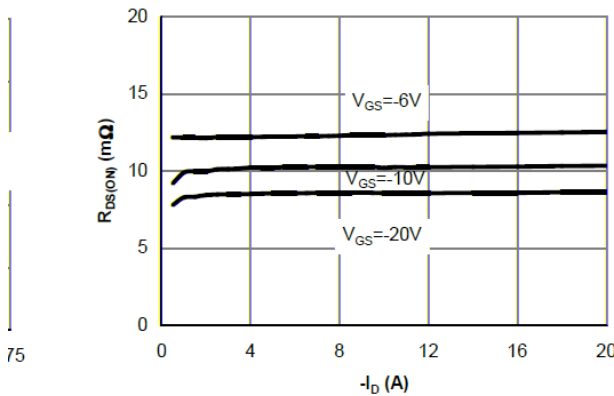


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

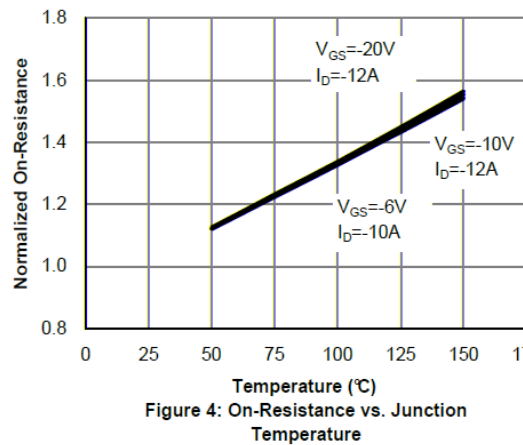


Figure 4: On-Resistance vs. Junction Temperature

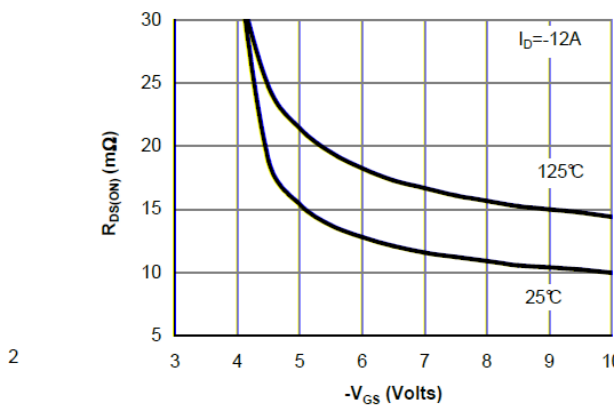


Figure 5: On-Resistance vs. Gate-Source Voltage

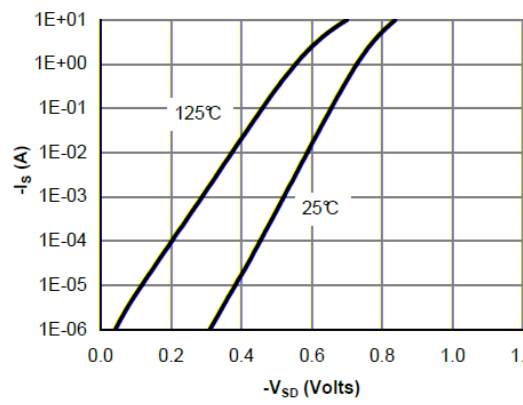
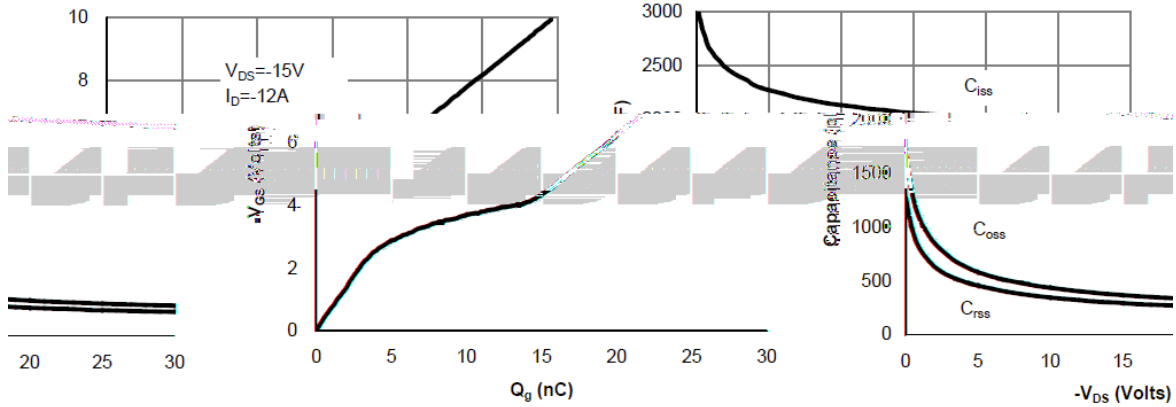


Figure 6: On-Resistance vs. Drain-Source Voltage

**TYPICAL CHARACTERISTICS**



Characteristics

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

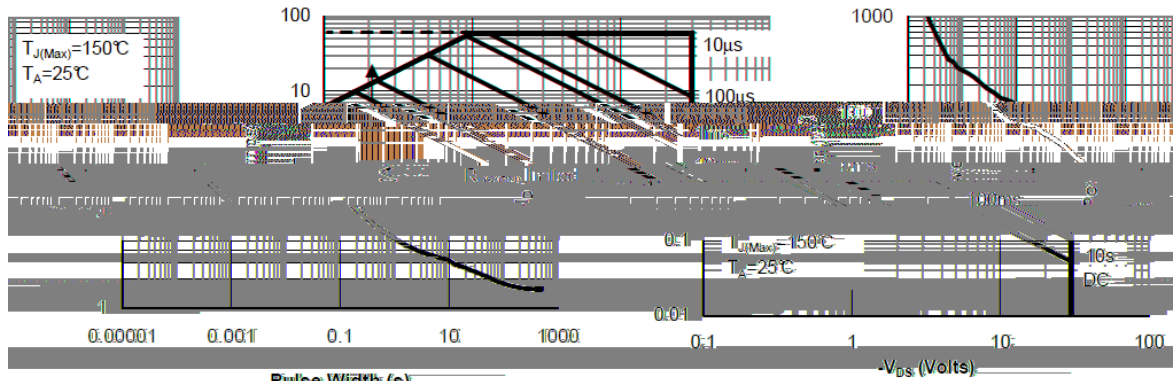


Figure 10: Single-Pulse Power Rating Junction-to-Ambient (Note E)

Figure 9: Maximum Forward-Biased-Safe Operating Area (Note E)

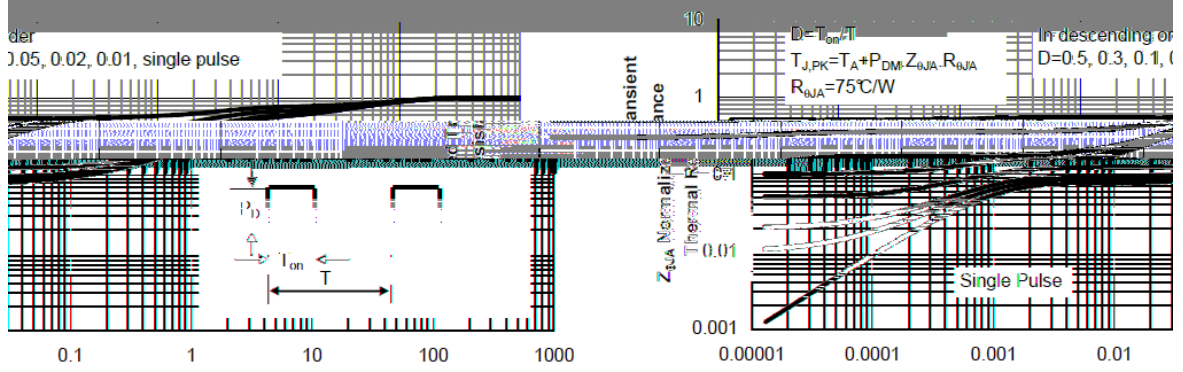
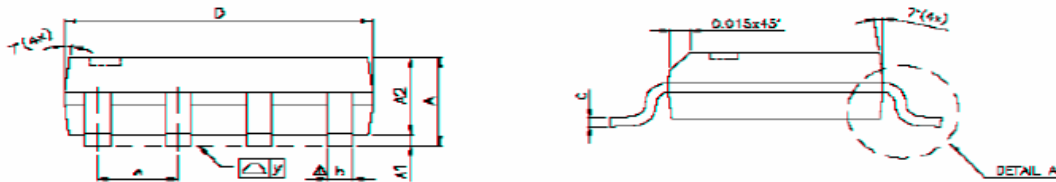
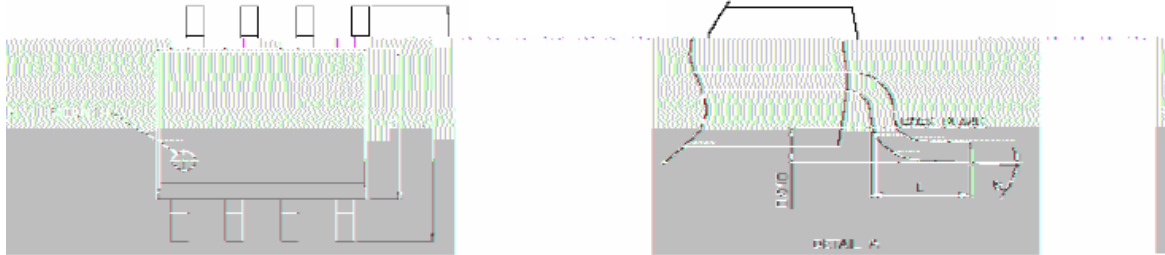


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

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**PACKAGE OUTLINE SOP-8P**



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A2	0.118	0.125	0.132	0.0047	0.0050	0.0052
B	0.013	0.016	0.020	0.0005	0.0006	0.0008
C	0.0075	0.008	0.0095	0.0003	0.0003	0.0004
D	0.189	0.191	0.195	0.0075	0.0076	0.0077
E	0.228	0.238	0.244	0.0090	0.0094	0.0096
E1	0.150	0.154	0.157	0.0059	0.0061	0.0062
e	—	0.050	—	—	0.0020	—
L	0.015	0.028	0.050	0.0006	0.0011	0.0020
$\Delta y$	—	—	0.003	—	—	0.0012
$\theta$	—	—	8°	—	—	8°